DFI-MINI 286
ADVANCED
PC-AT COMPATIBLE
SYSTEM BOARD
USERS MANUAL

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CONTENTS

INTRODUCTION

Thank you for purchasing the 286 AT SYSTEM BOARD. The 286 AT SYSTEM BOARD is a high quality, high reliability board and is among the most technologically advanced personal computer system boards ever produced. It is highly compatible with the established standard for high-performance computing, IBMs PC-AT. It is easy to set up and easy to use.

SPECIFICATIONS

- Normal/Turbo speed selected by hardware switch or keyboard switch.

- Normal speed can be 6MHz or 10MHz, selected by hardware jumper.

- 1 megabyte expansion capability on the system board.

- 16 megabyte expansion capability in the protected virtual address mode.

- Socket for 80287 math coprocessor.

- Rechargeable battery (Optional battery connector on system board for external battery connection.)

- 8 I/O expansion slots.

- CMOS clock and calendar circuit.

- LED display for power on and speed indication.

- External hardware reset for hardware and software debug purposes.

- 7 channel direct memory access (DMA).

- 16 levels of system interrupts.

- 3 programmable timers.

- Standard AT power supply connector.

- Speaker/keyboard connector.

- Speed indication connector.

CONNECTORS/JUMPERS

The system contains the following connectors:

- Keylock connector and power on indicator LED (J5)
- Two power supply connectors (PS1 and PS2)
- Keyboard connector (J15)
- Battery connector (J3 or J14)
- Speaker connector (J4)
- Normal/Turbo speed selection jumper (J10 or J12)
- Hardware reset connector (J2 or J13)
- Turbo LED connector (J1)
- Normal speed 6MHz/10MHz selection jumper (J11).
- 10MHz zero wait state enable/disable jumper (J8 & J9).
- Frequency indication connector (J6).

Connector/Jumper pinout usage

Power on LED and Keylock Connector (J5)

Pin	Assignment
1	LED power
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

- Power Supply Connectors (PS1 & PS2)

Power supply connector pin assignments are as follows:

Pin	Assignment	Connector
1	Power good	
2	+5Vdc	PS2
3	+12Vdc	
4	-12Vdc	
5	Ground	
6	Ground	
1	Ground	
2	Ground	PS1
3	-5Vdc	
4	+5Vdc	
5	+5Vdc	
6	+5Vdc	

- Keyboard Connector (J15)

The keyboard connector is a five-pin DIN 90-degree printed circuit board (PCB) mounting. The pin assignments are as follows:

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5Vdc

- Battery Connector (Only one of J3 or J14 being used.)

The pin assignments for keyed battery connector are as follows:

Pin	Assignment
1	6Vdc
2	Not used
3	Ground
4	Ground

Note: If you use an external battery which can't be recharged, please cut off the "s" indicator line on the right of POACH 1 chip set.

- Speaker Connector (J4)

The pin assignments for the speaker connector are as follows:

Pin	Function
1	Data out
2	Key
3	Ground
4	+5Vdc

- Hardware Reset Connector (Only one of J2 or J13 being used.)

The hardware reset is a 2-pin berg strip. The pin assignments are as follows:

Pin	Function
1	Ground
2	Selection pin

- Normal/Turbo speed selection jumper (Only one of J10 or J12 being used.)

The pin assignment for Normal/Turbo speed selection jumper are as follows:

Pin	Function
1	Turbo speed
2	Common
3	Normal speed

- Turbo LED Connector (J1)

The pin assignments for the turbo LED connector are as follows:

Pin	Function
1	LED indication out
2	+5Vdc

- Normal speed 6MHz/10MHz selection jumper (J11)

The pin assignments for the normal speed selection jumper are as follows:

Pin	Function
1	10MHz
2	Common
3	6MHz

- 10MHz zero wait state enable/disable jumper (Both J8 and J9 being set at same side.)

If your hard disk controller can not work with 10MHz zero wait enabled, please disable this function. Enabling 10MHz zero wait operation also enable the so called

early ALE mode, which result in different timing on the expansion slots.

Pin (J8, J9)	Function
1	Enabled
2	Common
3	Disabled

- Frequency indication connector (J6)

The frequency indication connector provides the current clock of speed.

Pin	Assignment
1	Clock output
2	+5Vdc
3	Key
4	Ground

DIP SWITCH SW1 SETTINGS

The table below explains the use and settings for each switch.

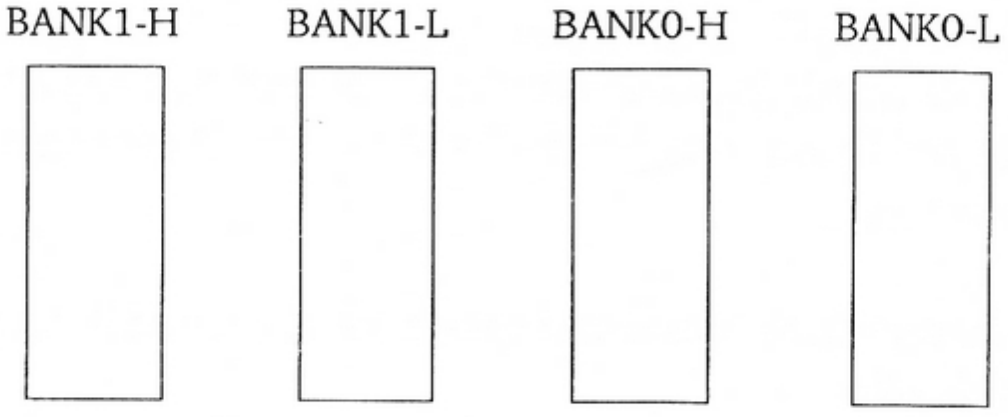
Switch	Position	Function
1	see Note 1	RAM size selection
2	see Note 1	RAM size selection
3	see Note 1	Base memory and expansion memory selection
4	ON	Reserved, must be off
	OFF	Operation mode
5	ON	Color primary display
	OFF	Monochrome primary display
6	ON	Auto switch to zero wait for normal speed
	OFF	Always one wait state
7	ON	256K ROM BIOS chips used
	OFF	128K ROM BIOS chips used
8	OFF	Reserved

Note 1: (* = don't care)

RAM size selection	Switch	Position
256K	1	ON
	2	ON
	3	*
512K	1	ON
	2	OFF
	3	*
640K	1	OFF
	2	ON
	3	*
1024K Base memory = 512K Expansion memory = 512K	1 2 3	OFF OFF OFF
1024K Base memory = 640K Expansion memory = 384K	1 2 3	OFF OFF ON

RAM CHIP INSTALLATION

The advanced mainboard allows choices of four RAM size: 256K, 512K, 640K and 1024K. First, find the location of the RAM Banks on the mainboard from the illustration figure below:



The table below explains the installation of the RAM chips on the mainboard:

RAM CHIPS

	BANK0-L	BANK0-H	BANK1-L	BANK1-H
256K RAM	4164x9	4164x9	4164x9	4164x9
512K RAM	41256x9	41256x9	No chips	No chips
640K RAM	41256x9	41256x9	4164x9	4164x9
1024K RAM	41256x9	41256x9	41256x9	41256x9

Note 1: Please see RAM size selection of the DIP switch settings before installing RAM chips.

Note 2: All the memory chips on the board should use 4164-10 or 41256-10.

CHANGING CLOCK SPEED

Keyboard switch for changing speed

- To switch from normal speed to turbo speed, just type

  CTRL, ALT, +

  In other words, hold down the CTRL and ALT keys, then while holding down, hit the "+" key. You'll see the turbo LED is ON.

- To change back to normal speed, hit the same keystroke combination:

  CTRL, ALT, +

  You'll see the turbo LED is OFF.

Hardware switch for changing speed

Only J10 or J12 is used for speed selection.

- If Pin 1 and Pin 2 is shorted, CPU is running at turbo speed. Turbo LED will be ON.

- If Pin 3 and Pin 2 is shorted, CPU is running at normal speed. Turbo LED will be OFF.

Note: Hardware change will override the software change. The connector should be left open if software change is desired.

TECHNICAL INFORMATION

Memory map

The 1M RAM on board can be set as follows: (Ref. see dip switch settings)

MODE 1: Base memory = 512KB
Expansion memory = 512KB

512K-512K MEMORY MAP

ADDRESS		MODE 1 NAME	FUNCTION
000000 07FFFF	to	512KB User RAM	System Board
080000 09FFFF	to	128KB User RAM	I/O Channel Memory
0A0000 0BFFFF	to	128KB Video RAM	Reserved for Graphics Display Buffer
0C0000 0DFFFF	to	128KB I/O System Board	Reserved for ROM on I/O Adapters
0E0000 0EFFFF	to	64KB Reserved on System Board	User ROM
0F0000 0FFFFF	to	64KB ROM on System Board	System BIOS ROM
100000 17FFFF	to	512KB User RAM	System Board
180000 FDFFFF	to	14720KB User RAM	I/O Channel Memory
FE0000 FEFFFF	to	64KB Reserved System Board	Duplicate Code Assignment at Address 0E0000
FF0000 FFFFFF	to	64KB ROM on System Board	Duplicate Code Assignment

MODE 2: Base memory = 640KB
Expansion memory = 384KB

ADDRESS		MODE 2 NAME	FUNCTION
000000 07FFFF	to	512KB User RAM	System Board Memory
080000 09FFFF	to	128KB User RAM	System Board Memory
0A0000 0BFFFF	to	128KB Video RAM	Reserved for Graphics Display Buffer
0C0000 0DFFFF	to	128KB I/O Expansion ROM	Reserved for ROM on I/O Adapters
0E0000 0EFFFF	to	64KB Reserved on System Board	User ROM
0F0000 0FFFFF	to	64KB ROM on System Board	System BIOS ROM
100000 15FFFF	to	384KB User RAM	System Board Memory
160000 FDFFFF	to	14848KB User RAM	I/O Channel Memory
FE0000 FEFFFF	to	64KB Reserved System Board	Duplicate Code Assignment at Address 0E0000
FF0000 FFFFFF	to	64KB ROM on System Board	Duplicate Code Assignment at Address 0F0000

I/O Address Map

ADDRESS (HEX)	DEVICE
000-01F	DMA Controller 1, 8237
020-03F	Interrupt Controller 1, 8259, Master
040-05F	Timer, 8254
060-06F	Keyboard Controller, 8742
070-07F	Real Time Clock, NMI (non-maskable interrupt) mask
080-09F	DMA Page Registers, 74LS612
0A0-0BF	Interrupt Controller 2, 8259
0C0-0DF	DMA Controller 2, 8237
0F0	Clear Match Coprocessor 80287 Busy
0F1	Reset Match Coprocessor 80287
0F8-0FF	Match Coprocessor 80287
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

System Timers

The system has three programmable timer/counters controlled by an 8254 timer/counter on the POACH 2 chip set and defined as channels 0 through 2:

Channel 0	System Timer
GATE 0	Tied on
CLK IN	1.190MHz OSC
CLK OUT 0	8259 IRQ0
Channel 1	Refresh Request Generator
GATE 1	Tied on
CLK IN 1	1.190MHz OSC
CLK OUT 1	Request Refresh Cycle

Note: Channel 1 is programmed to generate a 15-microsecond period signal.

Channel 2	Tone Generation for Speaker
GATE 2	Controlled by bit 0 of port hex 61 PPI bit
CLK IN 2	1.190MHz OSC
CLK OUT 2	Used to drive the speaker

The 8254 Timer/Counter is treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters, the fourth is a control register for mode programming.

System Interrupts

Sixteen levels of system interrupts are provided by the 80286 NMI and two 8259 Interrupt Controller on the

POACH 1 chip set. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		Parity or I/O Channel Check
Interrupt CTLR 1	Controllers CTLR 2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Realtime Clock Interrupt
	IRQ9	Software Redirected to INT OAH (IRQ 2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1

DMA Channels

- DMA Channels

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

- DMA Page Register

Page Register	I/O Hex Address
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

Real Time Clock and CMOS RAM

The CMOS RAM on the POACH 1 chip set (146818) contains the real-time clock and 64 bytes of CMOS RAM, which keeps configuration information when power is off. The following figures show the CMOS RAM addresses.

Addresses	Description
00-0D	* Real-time clock information
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte-drives A and B
11	Reserved
12	Fixed disk type byte-drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

CMOS RAM Address Map

Byte	Function	Address
0	Seconds	0C
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
14	Status Register D	0D

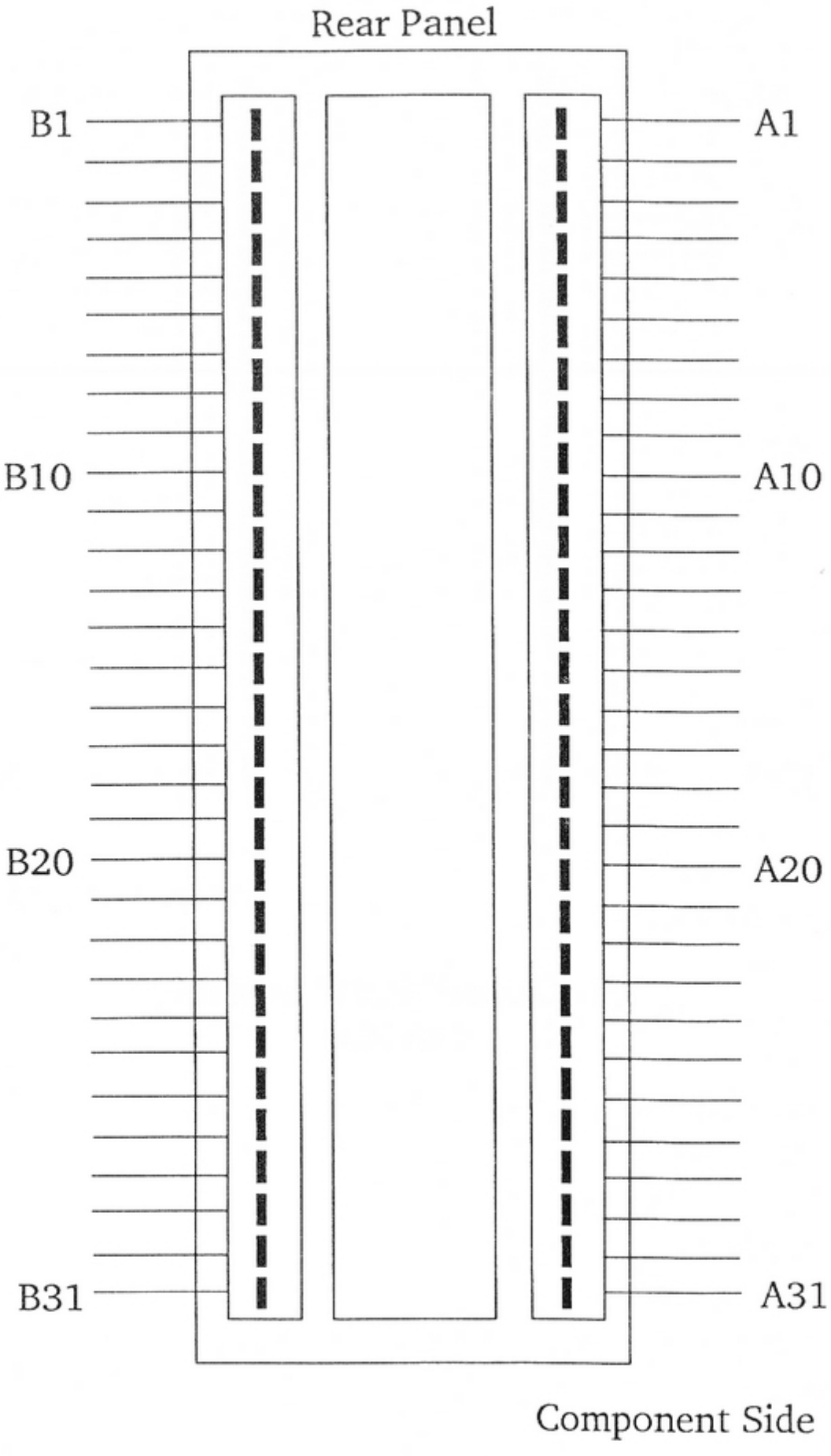
Real-Time Clock Information
(addresses 00-0D)

I/O Connector Channels

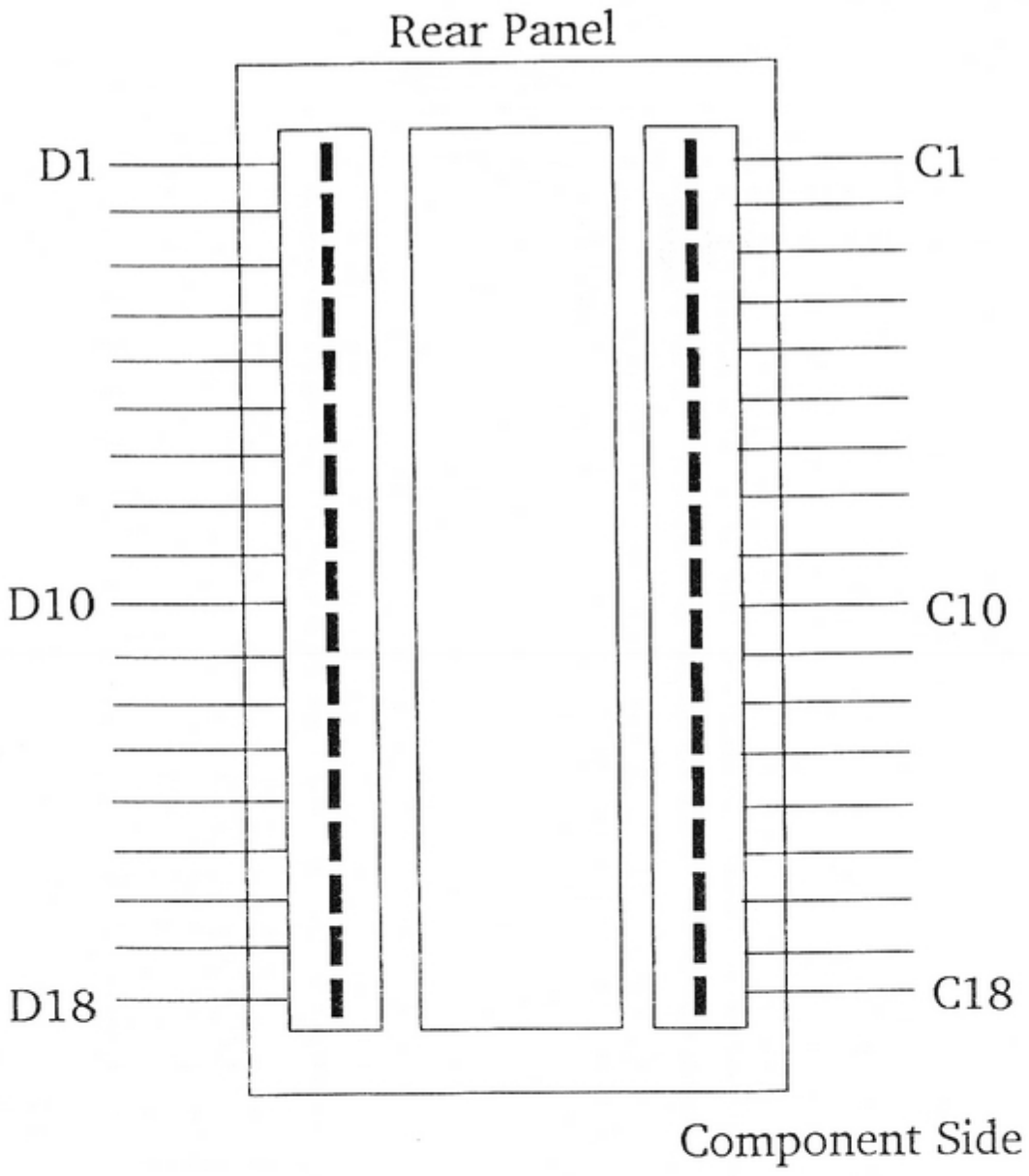
THE I/O CHANNEL SUPPORTS:

- I/O address space from hex 100 to hex 3FF
- Selection of data access (either 8 or 16 bit)
- 24 bit memory addresses (16MB)
- Interrupts
- DMA channels
- Refresh of system memory from channel microprocessors

The following figures show the pin numbering for 62-pin and 36-pin I/O channel connectors:



I/O Channel Pin Numbering
(62 Pin)



I/O Channel Pin Numbering
(36 Pin)

The I/O channel pin assignments:

I/O Pin	Signal Name	I/O
A 1	-I/O CH CK	I
A 2	SD7	I/O
A 3	SD6	I/O
A 4	SD5	I/O
A 5	SD4	I/O
A 6	SD3	I/O
A 7	SD2	I/O
A 8	SD1	I/O
A 9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Pin	Signal Name	I/O
B 1	GND	Ground
B 2	RESET DRV	O
B 3	+5Vdc	Power
B 4	IRQ9	I
B 5	-5Vdc	Power
B 6	DRQ2	I
B 7	-12Vdc	Power
B 8	OWS	I
B 9	+12Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	O
B16	DRQ3	I
B17	-DACK1	O
B18	DRQ1	I
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5Vdc	Power
B30	OSC	O
B31	GND	Ground

I/O Pin	Signal Name	I/O
C 1	SBHE	I/O
C 2	LA23	I/O
C 3	LA22	I/O
C 4	LA21	I/O
C 5	LA20	I/O
C 6	LA19	I/O
C 7	LA18	I/O
C 8	LA17	I/O
C 9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O Pin	Signal Name	I/O
D 1	-MEM CS16	I
D 2	-I/O CS16	I
D 3	IRQ10	I
D 4	IRQ11	I
D 5	IRQ12	I
D 6	IRQ15	I
D 7	IRQ14	I
D 8	-DACK0	O
D 9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5Vdc	Power
D17	-MASTER	I
D18	GND	Ground

Note: I/O slots consist of eight 62-pin and six 36-pin edge connector sockets. Two positions on the I/O channel do not have the 36-pin connector. These positions can only support a 62-pin I/O bus adapter.

REFERENCE BOOKS

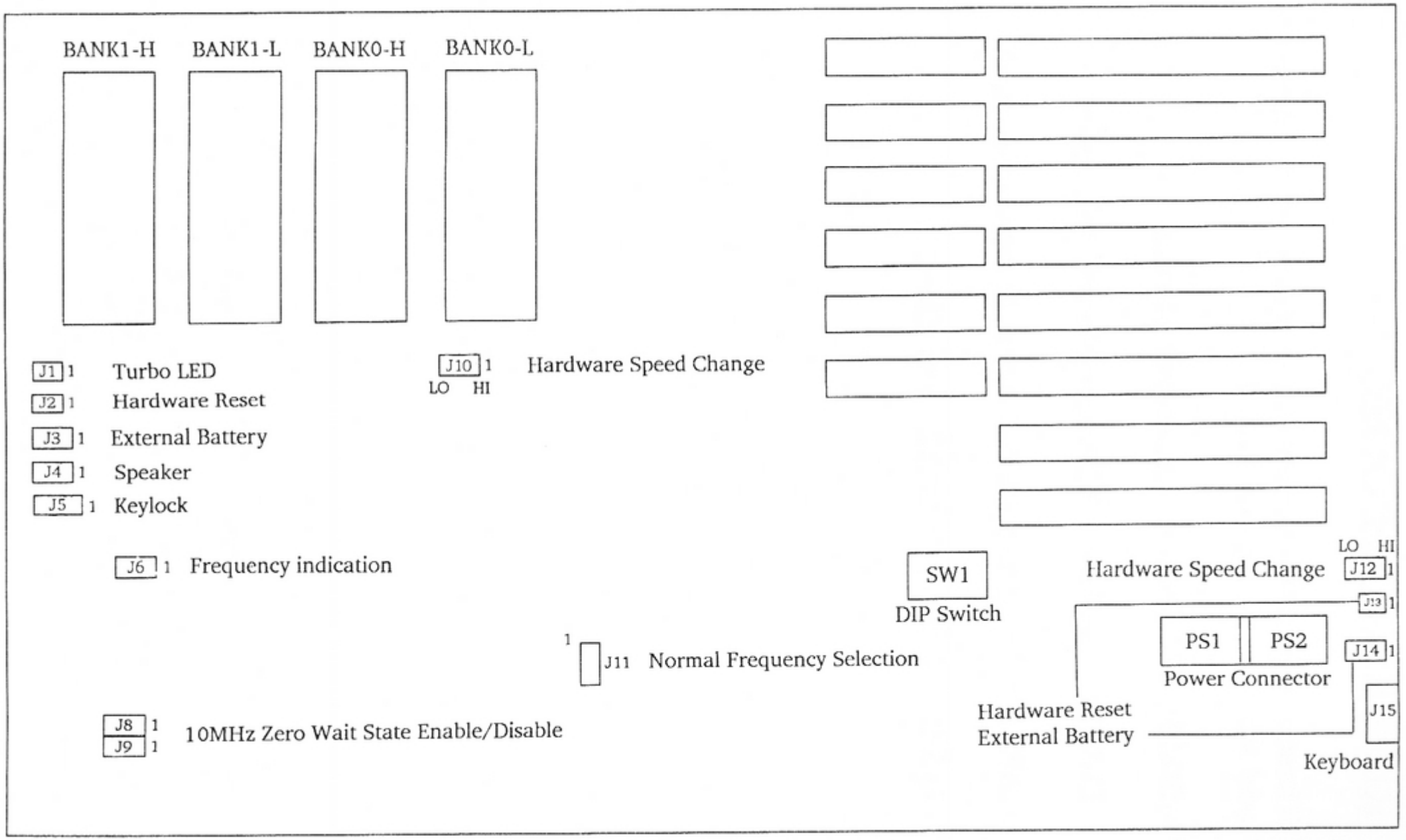
These are the reference books recommended for hardware and software system engineers:

- IBM PC/AT Technical Reference Manual

- iAPX 286 Hardware Reference Manual from Intel

- iAPX 286 Programmers Reference Manual from Intel

- ZyMOS POACH1/POACH2 Data Sheet


BANK1-H
BANK1-L
BANK0-H
BANK0-L
J1 1 Turbo LED
J2 1 Hardware Reset
J3 1 External Battery
J4 1 Speaker
J5 1 Keylock
J6 1 Frequency indication
J10 1
LO HI
Hardware Speed Change
SW1
DIP Switch
LO HI
Hardware Speed Change
J12 1
J13 1
PS1
PS2
Power Connector
J14 1
J15
Keyboard
Hardware Reset
External Battery
1
J11 Normal Frequency Selection
J8 1
J9 1
10MHz Zero Wait State Enable/Disable